

High Performance

MDUSTRA

COMPUTERS

Simultaneous

PCI Formfactor

ACQ32PCI

- ñ 32 Channels, 16 bit 250kSPS
- ñ Offset and Gain Calibration for good DC spec
- ñ Input Buffer Amp
- ñ Great AC Specs
- ñ Range of termination options

ACQ16PCI

- ñ Options 16 x 1.8MSPS to 2 x 10MSPS, 14 bit
- Buffered Differential Input
- ñ Good AC Specs.

CompactPCI Formfactor

ACQ32CPCI

- ñ Single slot 6U, base board + mezzanine, large useable board area
- ñ 32 Channels, 16 bit 250kSPS
- ñ Offset and Gain Calibration for good DC spec, Great AC Specs.

M1 Mezzanine

ñ Low cost single ended, with overvoltage

M2 Mezzanine

n Differential inputs, high gain PGA, Anti-Alias, medium speed.

M3 Mezzanine

- n Differential inputs, PGA, Anti-Alias, high speed.
- Wide Common Mode Range +/-90V Operation

Simultaneous Channels

ADC per Channel Architecture

ñ no mux bottleneck, no expensive sample and hold.

Conventional SAR or Flash Convertors take point samples.

ñ no time averaging as seen with sigma delta convertors.

External, Internal and Derived Clock options coupled by asynchronous logic ensure all Convertors clock together

External Trigger events inserted in digital data stream for correct synchronization.

Simultaneous Systems

Clock and Trigger Signals can be bussed between boards

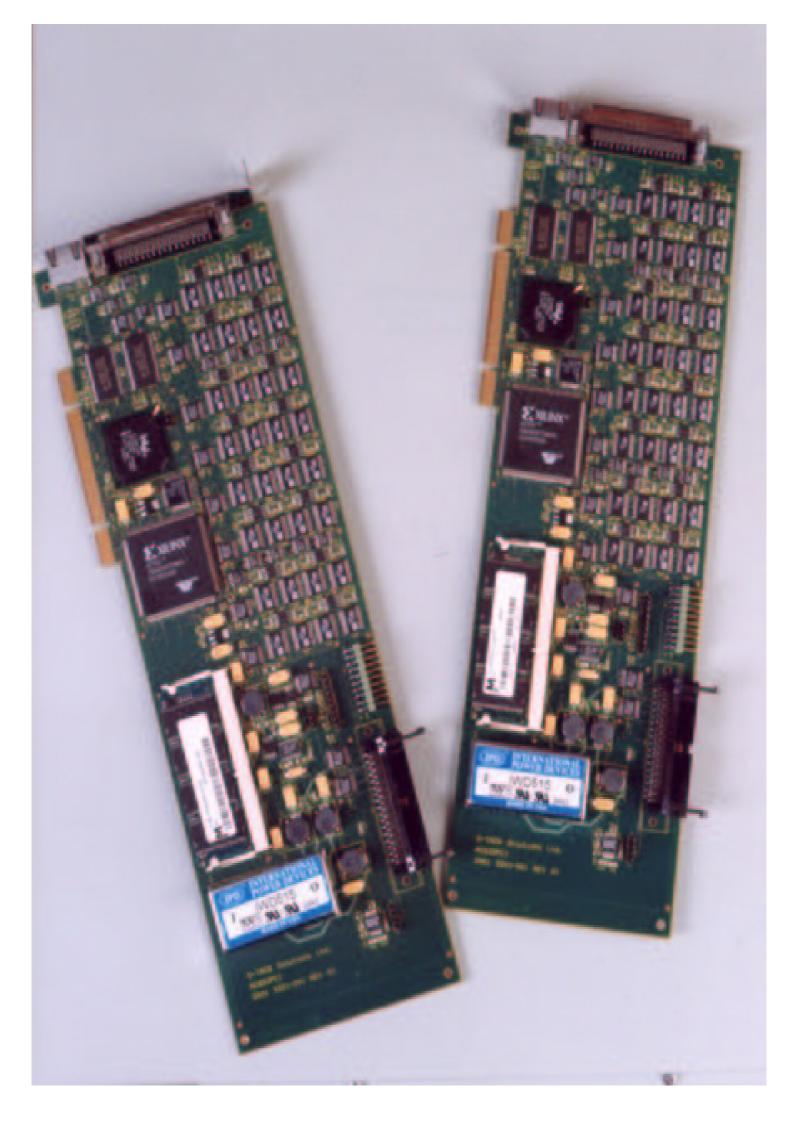
- ñ Ribbon cable on PCI
- ñ PXI backplane bus lines on Compact PCI

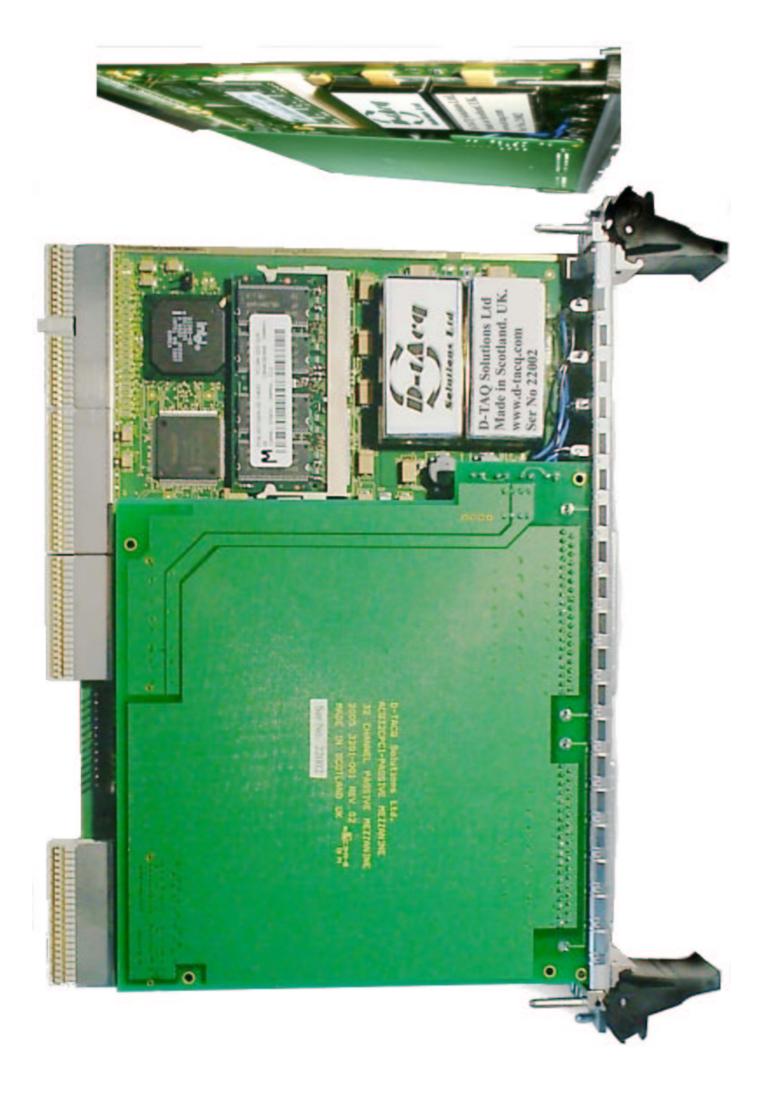
Multiple Clocking Options

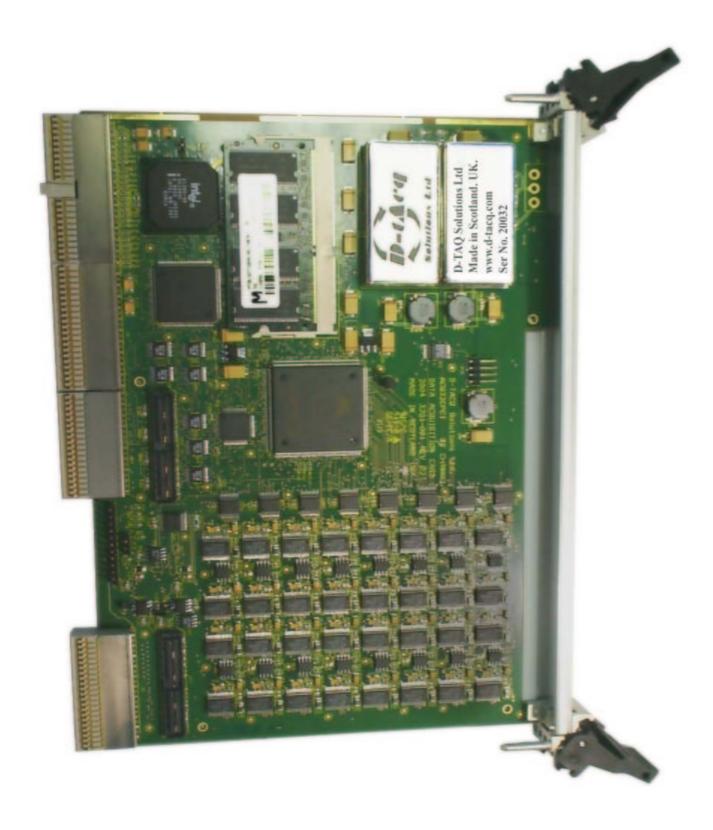
- Front panel clock (opto-isolated on ACQ32CPCI) can be divided and output to all boards in chassis
- n Internal Clock on one board can master other boards in chassis

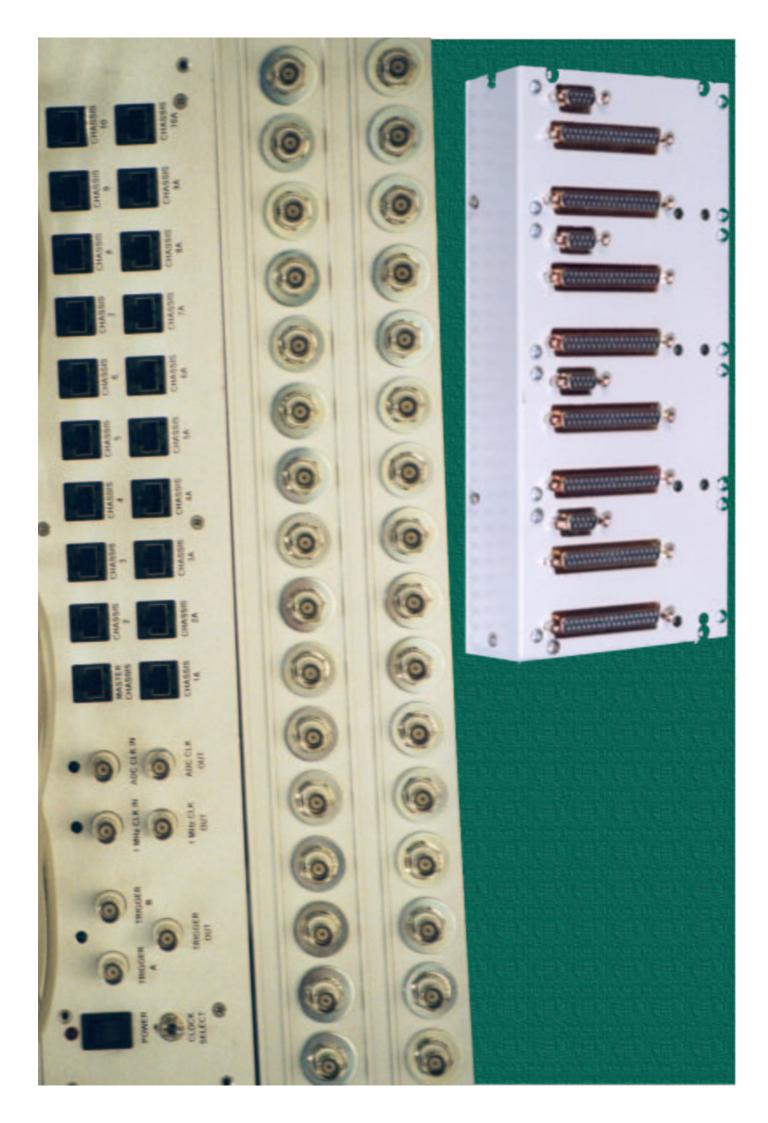
Simultaneous between chassis

^ñ Clock and trigger distributor panel.







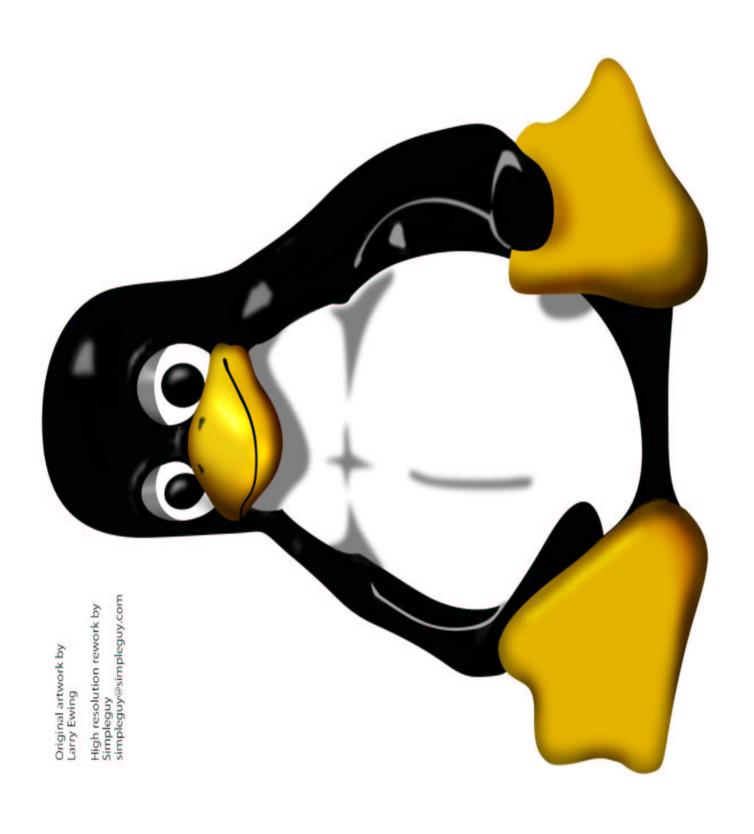




Intelligence

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Flexibility



Open System with Realtime and Control Capability

Embedded System

Onboard uP

- ñ 230MIPS, low cost Strong Arm
- ñ Self test, set up, many options possible

Big FPGA

- ñ Fast, wide, deep data path from ADC
- ñ Many triggering options

Deep Memory

- ñ 128MB fitted as standard. 8 sec transient 250kSPS x 32 Channels.
- ñ High performance DMA upload over PCI.

In System Upgradeable

n uP and FPGA code in flash memory. Remote upgrades routine!

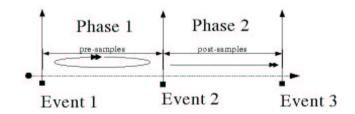
Flexible Triggering

Pre and Post

n User specifies pre, post length to limit of onboard memory. Falling edge digital trigger

Generalized Phase Event Model

- ñ Two phase, three event model.
- ñ Event can be any digital, any sense, soft or null



Output Waveform Functions

^ñ 2 Channels analog to 1MSPS, 8 bits digital, concurrent with capture, independent clockand trigger.

Analog Triggering

ñ Level and threshold, any channel at subrate. Any pair of channels at 2MSPS on ACQ16.

Open System





Linux

- ñ Open Source Driver and Test Apps supplied free to customers.
- ñ Highly Scriptable.
- ñ Open and documented interface to driver.

IP Networking

- ñ Multithreaded control and data server
- n Open Source, Easy to use, portable UI client app
- Web based status monitoring

MDSplus

Fully supported and used with MDSplus, the system of choice for handling very large data sets.









Realtime and Control

Subrate Streaming

Stream a subset of the data over pci for monitoring or control during local data capture.

High Throughput Streaming

Note The Stream full rate data (16x1MSPS) over pci to host memory for deeper store or real time analysis.

Low Latency Control

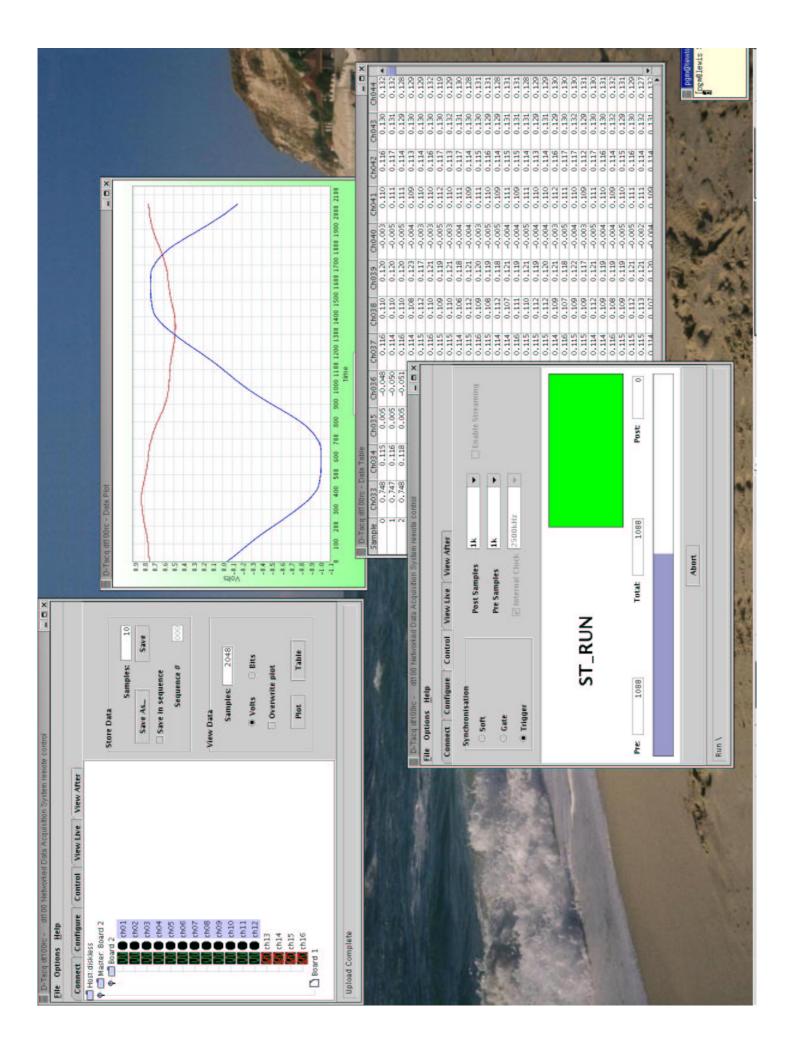
Note to delivery of 128 channels data to host memory).

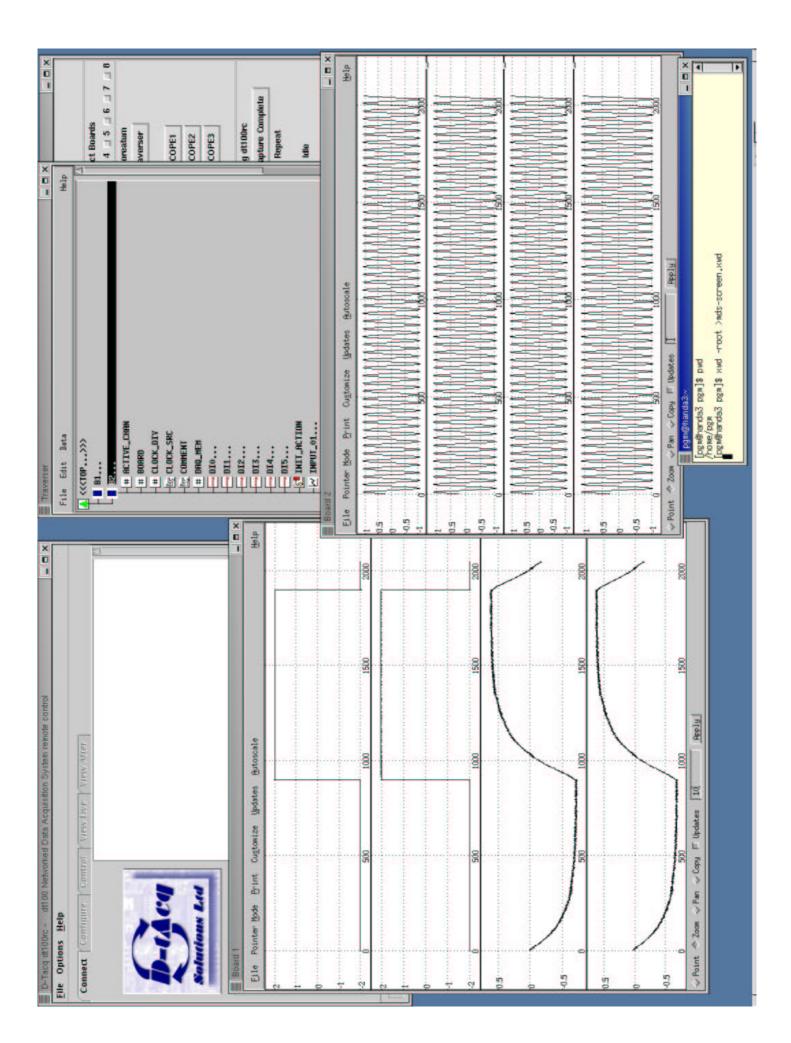
Very tight onboard control loops possible

necessor Custom control apps using the onboard uP and FPGA coprocessor.









www.d-tacq.com

