Intelligence Means Flexibility: ACQ32/16 Operating Modes

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1 Overview

The D-TACQ intelligent board architecture implemented on ACQ32PCI/ ACQ32CPCI/ ACQ16PCI uses a large Field Programmable Gate Array (FPGA) and a powerful, but low power, low cost microprocessor (uP) on board to manage data flows.

This means that the data path of the board is almost entirely configured by onboard firmware, resulting in great flexibility. A number of different operating modes have been developed in response to end user requirements.

The architecture calls for a fast, wide data path from the ADC array to a FIFO implemented in the FPGA. Data then flows from the FIFO to one of a variety of destinations as determined by the operating mode. Typical use is to transfer the data directly to the deep onboard transient memory; however use of the microprocessor enables a large number of possibilities. All uP and FPGA configuration data is held in FLASH memory, the system is in-system programmable; this can be performed remotely; field upgrades to add new features are performed regularly.

2 Transient Captures

The large onboard memory feature of the boards makes a transient capture extremely simple to perform, especially as there is no real time control demand made on the host computer.

2.1 Simplest Case

The simplest transient capture is a “SOFT TRANSIENT” - on soft trigger, data is captured to local memory. This is useful for testing board and wiring, but in general the sampling needs to be synchronised to some external event.

The most common Pre and Post Trigger mode is “TRIGGERED CONTINUOUS” where user commands specify pre trigger capture length, post trigger capture length. On an "ARM" command, the board captures data continuously to a cyclic pre- buffer. The trigger, normally a falling external digital edge, causes transition to the Post capture mode; once the specified number of Post samples has been acquired, then capture is terminated.

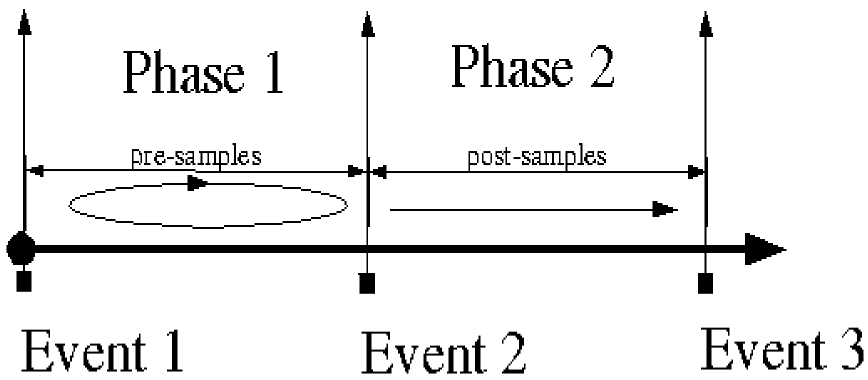
Viewing, upload or store of data is simply accomplished by reading standard devices. A high performance DMA mode is available, either via a sample application or linked to a user program.

2.2 General Case

The triggering model is also available as a general 2 phase, 3 event model. Phase 1 is the cyclic Pre-capture, Phase 2 is the one shot post capture. The spanning Events are completely generic, and can be any digital input line, any sense. Analog threshold triggers are also specified.

This General Phase Event Model (GPEM) may be extended beyond the Analog Input (AI) function to include, on ACQ32, Analog Output (AO) and Digital Output (DO) functions as well.

Each function may, under software control either share clocks and triggers with other functions, or use independent clocks and triggers. The system is completely generic.



2.3 Digital Trigger

ACQ32/16 offers six digital input lines that can be used as external clocks and triggers.

The Compact PCI board offers a flexible switched routing scheme to route synchronisation signals to any of Front Panel (Mezzanine) Input (MI), Mezzanine Output (MO), Rear IO (J5) and backplane signaling buses (PXI_TRIG)..

The PCI boards allow common trigger connection via a top of board ribbon cable.

2.4 Clocking

The boards can operate off either internal or external clocks. The internal clock is the best fit of two internal fast clocks (66 and 44 MHz), divided by a counter. The external clock may optionally be divided by a counter, used on board and retransmitted off board.

The equipment is designed to run multiple boards in a chassis, completely simultaneously. Only one clock and trigger connection is needed per chassis. D-TACQ also offers a multi chassis solution in the shape of a clock and trigger distributor module, that allows up to 10 chassis to be synchronised.

2.5 Analog Trigger

A generic trigger is available where every input is scanned against user specified thresholds and direction, implementing a rising/falling edge trigger, on any and all channels. The scan interval of this trigger is limited by the data rate of the capture in question, and, as the data rate, or the number of channels with set thresholds rises, so will the sample interval. Given the deep memory buffers available, and assuming a slow moving trigger condition, this may be an acceptable solution. Alternatively, there is a fast two channel trigger that will guarantee to examine every sample for trigger purposes on any pair of channels on a twelve channel ACQ16 up to 2 MSPS. Other fast trigger functions can be implemented as required.

2.6 Output Functions

ACQ32 has two 16 bit Analog Output (AO) channels. These can be driven immediately to values specified by command over PCI, or via an arbitrary waveform. The waveform is preloaded, and the length of the waveform is limited only by the amount of onboard memory. The 128MB data storage memory is shared between the AI and AO functions for this purpose.

Eight general purpose Digital Output (DO) lines are also available, and in a similar way to AO, these may either be driven directly via PCI command or via an arbitrary pattern. The pattern is loaded as a series of 32 bit words, 24 bit clock count, 8 bit value. This accommodates complex timing patterns in a small amount of memory.

Both output waveform functions are compatible with both the simple and generic modes of operation. In the simple mode, the AO function is most useful for loopback testing. In the generic mode of operation, the output functions operate with the same controls as the AI function. In the most general case, all three functions, AI, AO, DO can operate off independent clocks and triggers; but this is not mandated, for example a common scenario is to operate AO, DO off an external 1MHz clock. This clock is divided by 4 onboard and redistributed as a 250KHz AI clock. Typically, all the functions share the same E2 event.

3 Control

The intelligent architecture enables a number of possibilities for control.

3.1 Low Latency via PCI bus

ACQ32 can operate in a low latency acquisition mode. In this case the onboard uP is closely synchronised to commands from the host computer. The host computer allocates and locks down a region of PCI slave memory in its address space, and passes this address to the ACQ32. The ACQ32 is typically fed with an external 1MHz clock and a gate signal. On the first clock after the gate, ACQ32 captures a (32 channel) sample of data and transfers this via PCI to the host memory. The ACQ32 also implements a 32 bit external clock count, and information about the clock count at time of conversion, the time to transfer the data to host memory and the current time is available to the host computer.

Measurements show that on a system with one ACQ32, time from clock to 32 samples copied into memory is of the order of 8 usec, on a 4 board system, time from sample clock to 128 samples copied into memory is about 12 usec.

These tight latencies are enabled by: fast ADC conversion, data is available in 2.5 usec, and an efficient DMA controller with preloaded setup. Time on the PCI bus is very short, and the 4 board case works well because of most of the process delays occur on each board in parallel, and when it comes to contention on the PCI bus for the final transfer phase, we have 4 DMA controllers, buffers loaded, waiting for a bus grant, this process is entirely down to hardware switching and is clearly very efficient.

3.2 On Board control loops

The combination of a 200MIPs general purpose CPU and a large FPGA co-processor, on board inputs and outputs makes implementing extremely low latency control loops feasible. Total latency due to input and output can be 5 usec or less, so assuming for example, a comparable calculation taking 5 usec, then a 100kHz rep rate with a 10 usec latency is possible.

4 Streaming

Full rate data is streamed direct from capture FIFO to host PCI memory. Testing on ACQ16 shows 16x1MSPS sustained to be achievable. 32x250kSPS on ACQ32 is also possible. Because the streaming is “target push”, DMA from target board to host memory, this operation imposes little load on the host cpu, leaving most of the available cpu power available for storing data direct to local disk, streaming out via a network port or for real time control. A sample application “htstream” is supplied with the source code.

5 Hybrid Operations: Subrate Streaming

During a regular full rate capture to cyclic buffer in onboard memory, the hybrid model allows streaming a subset of data to PCI bus; This subset may be used for realtime monitoring or control purposes. The implementation is entirely in microprocessor firmware on the ACQ32 and currently the full rate capture is limited to 150kSPS. An Enhanced model is planned, dedicating two FIFO's in the FPGA, one FIFO to transfer full rate data (32 x 250kSPS) to local memory as normal, a second FIFO to transfer subrate data out via the PCI bus. This subrate data may also be a mean of several samples for lower noise, or adjusted by some simple unit conversion function.